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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,007	MCADAMS, MARK ALAN	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/4/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-18,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-18,23 and 24* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment dated 10/04/2004.

Claims 1, 3, 4, 8, 11-17, 23 and 24 were amended by the applicant.

Claims 2, 10, 19-22 and 25 were cancelled by the applicant.

Claims 1, 3-9, 11-18, 23 and 24 are pending in this action.

Response to Amendment

1. In view of the applicant's changes to the Specification, the examiner's objections to said Specification are withdrawn, and the changes are approved.

2. In view of the applicant's amended drawings, the examiner withdraws the objections to said drawings and hereby approves the new drawings.

3. In view of the applicant's changes to Claims 1, 3, 4, 16, 19 and 23, the examiner has withdrawn the objections to said claims. The examiner notes that only item 14 of the examiner's previous office action was corrected by the applicant in regard to Claim 23.

4. In view of the applicant's changes to Claim 23, the examiner notes that the applicant failed to change the claim in line 9 as follows; "when the integrate~~s~~[d] circuit". The examiner maintains the objection to this informality as outlined in item 15 of the examiner's previous office action.

Response to Arguments

5. Applicant's arguments with respect to Claims 1, 3-9, and 11-18 have been considered but are moot in view of the new grounds of rejection. However, in the

interest of clarification, the examiner is providing the following rebuttals to the applicant's arguments re: Claims 1, 3-9 and 11-18:

The applicant argued (page 10, paragraphs 3 and 4) that in Bhattacharya, multiple TAPs are used. But the examiner used the reference of Bhattacharya strictly for the purpose of teaching a 5th JTAG compatible conductor, TRST. This conductor is compatible with JTAG while either being present or absent from an application of the standard. This optional conductor, being present in Bhattacharya but absent in Jabar, is taught by Bhattacharya. Also argued is that TRST added to Jabar would not make Jabar JTAG compliant but the examiner disgrees. Jabar is JTAG compliant (column 4 lines 8-11), and TRST, being a 5th optional JTAG compliant signal, does not render Jabar non-compliant. The applicant argues that, with 4 internally generated clock lines in Jabar, the reference would not have any lines left for TRST. But the internally generated lines do not add to the 4 lines of Jabar, thus the JTAG interface of Jabar, including TRST of Bhattacharya, would be compliant with the 5 line JTAG standard. The applicant on page 10 last paragraph to page 11 1st paragraph argues that in Claims 10-13, Jin does not have the same motivation to be combined with Jabar because it is not the same as the motivation of Jabar and the applicant. The motivation for Jin only serves to provide the reference required to achieve a teaching which would reject the applicant, and does not have to match the motivation of either the applicant nor the prime reference. Also, although Jabar has worked out a different method for internal control of each core, one may still learn from, and adopt, a different approach to internal control as taught by Jin. Finally, as per Claims 14-16, the applicant argues that the

motivation for Sim teaches away from JTAG compliance, but the examiner disagrees. Column 1 lines 31-45 teach that the invention may use JTAG even though it would add to overhead. Further, the invention increases core testability, JTAG or not, (column 2 lines 9-12). One with ordinary skill in the art would be motivated to increase core testability, particularly while applying JTAG requirements (which may be used) in order to effectively test multiple cores.

6. In regard to Claims 23 and 24, applicant's arguments filed 10/04/2004 have been fully considered but they are not persuasive. As per the examiner's original office action, the following is the basis of rejection for Claims 23 and 24 under 35 USC 103 over Jaber, in view of Bhattacharya and Jin:

As per Claim 23:

Jaber teaches the system for testing one or more of multiple circuit modules embedded in an integrated circuit, comprising: a test controller for accepting serial data and control signals from outside the integrated circuit, using four conductors including a clock conductor (FIG.5 TCK), a test mode conductor (FIG.5 TMS), a data in conductor (FIG.5 TDI) and a data out conductor (FIG.5 TDO), one or more multiple boundary scan registers (FIG.5 SCAN STRING 0...n), each boundary scan register corresponding to one of the circuit modules (see Absract), each boundary scan register providing input to the corresponding circuit module from the test controller when the integrated circuit is in a test mode and from an operating input when in the integrates circuit is in an operating mode (FIG.7 70 and FIG.6 DATA IN). Jaber however fails to teach a fifth optional 1149.1 standard conductor, a reset conductor. In an analogous art, Bhattacharya

teaches this feature (FIG.7 TRST*). One with ordinary skill in the art would find it to be an obvious choice to include the fifth conductor in a JTAG compatible interface as taught by Bhattacharya into the JTAG interface of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1 while providing reset function to embedded circuits. Bhattacharya, in column 1 lines 55-61 and column 2 lines 1-6 states the need to be JTAG compliant and an advantage of that invention as being compliant in that respect. Jaber also teaches conductors for the test controller to communicate with the boundary scan registers, the conductors including a data-in line (FIG.5 TDI), a data-out line (FIG.5 TDO), a clock line (FIG.5 49), and an input application line to indicate that input data in the boundary scan register is to be applied to the inputs of the circuit module (FIG.5 51 and MASTER TCK as per column 7 lines 54-67 and column 8 lines 1-11). Jaber fails to teach two additional lines; a mode line to indicate whether the integrated circuit module is in test mode or operating mode, and an output data capture line indicating that output from the circuit module is to be captured. But in the analogous art of Jin, these two signals are featured in FIG.1C as MODE and UPDATEDR. One with ordinary skill in the art would find it to be an obvious choice to include the six conductors above in a master/slave arrangement as taught by Jin, into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several embedded circuits. Jin, in column 2 lines 63-66 and column 2 lines 1-6 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's timing characteristics. One with ordinary skill in

the art at the time of the invention, motivated by Bhattacharya and Jin, would combine the two references for their features while maintaining JTAG compliance.

As per Claim 24:

Jaber further teaches the method of claim 23 in which the test controller includes logic for accepting commands and data formatted in a JTAG protocol (see Abstract and column 4 lines 8-20). And in view of the motivation previously stated, the claim is rejected.

The applicant argues, on page 9 and 10 of the amendment, that the JTAG of Jabar teaches transmitting 4 clock signals to each scan element and a "stop control". But these signals are internally generated by the clock circuit 51 of FIG.5, and do not change the JTAG compliance of the external TAP conductors. Also argued that TMS is used as a clock line, but the examiner answers that the TMS line of Jabar is a dual purpose line that anticipates the limitations of the applicant's Claim 23. Since the TMS line is JTAG compliant (Jabar, column 4 lines 8-20), any supplemental use of TMS during TEST to control the MASTER CLOCK (A, B) in the FIG.5 clock circuit 51 simply serves to satisfy the rejection of the claim by providing teachings for either limitation or both. The applicant presented no other argument for the Claims 23 and 24. The examiner reminds the applicant that if the references fail to show certain features of an applicant's invention, it is noted that the features upon which applicant may rely upon, if not recited in a rejected claim, are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, the examiner maintains the rejections of Claims 23 and 24 under 35 USC 103.

Claim Rejections - 35 USC § 103

Claims 1, 3-9, and 11-18

7. Claims 1, 3-7, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jabar, U.S. Patent No. 6028983, and in view of Bhattacharya, U.S. Patent No. 6425100.

As per Claims 1, 17 and 18:

Jaber teaches a method of testing a circuit module embedded in an integrated circuit (see Abstract), at least some of the pins of the circuit module not being directly connected to a pin of the integrated circuit, the method comprising: communicating test commands and data using a board-level test protocol through a test interface (column 4 lines 59-67 and column 5 lines 1-19) by; scanning test vector data into a scan chain associated with the inputs of the circuit module (FIG.7 60, 62, 64, 66); applying the test vector data in the scan chain as input to the circuit module (FIG.7 68); and retrieving the output of the circuit module through the scan chain to the test interface (FIG.7 72, 74, 76 and column 4 lines 8-35). Jaber teaches the method of claim 1 and system of Claim 8 in which communicating test commands and data includes communicating test commands and data from off the integrated circuit using four conductors including a clock conductor (FIG.5 TCK), a test mode conductor (FIG.5 TMS), a data in conductor (FIG.5 TDI) and a data out conductor (FIG.5 TDO). Jaber however fails to teach a fifth optional 1149.1 standard conductor, a reset conductor as claimed in Claim 2 of the application. In an analogous art, Bhattacharya teaches this feature (FIG.7 TRST*). One

with ordinary skill in the art would find it to be an obvious choice to include the fifth conductor in a JTAG compatible interface as taught by Bhattacharya into the JTAG interface of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1 while employing an external reset capability. Bhattacharya, in column 1 lines 55-61 and column 2 lines 1-6 states the need to be JTAG compliant and an advantage of that invention as being compliant in that respect. One with ordinary skill in the art at the time of the invention, motivated by Bhattacharya, would combine the two references in order to apply reset from an external source.

As per Claim 3:

Jaber further teaches the method of claim 1 further comprising converting a test vector into a series of JTAG protocol test commands and data, the JTAG command including a user defined command (FIG.5 44) for defining an address for a circuit module (column 6 lines 26-64). And in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

Jaber further teaches the method of claim 3 in which converting a test vector includes maintaining timing relationships actions initiated by the test commands (see FIG.7 60-76). And in view of the motivation previously stated, the claim is rejected.

As per Claim 5:

Jaber further teaches the method of claim 1 in which scanning test vector data into a scan chain includes scanning the test vector data to a single boundary scan register (see Abstract), the single boundary scan register being associated with the

circuit module under test (FIG.7 70). And in view of the motivation previously stated, the claim is rejected.

As per Claim 6:

Jaber further teaches the method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary scan register to the test interface without scanning the output through a second boundary scan ring (see Abstract and FIG.4). And in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

Jaber further teaches the method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary scan register through at least one dedicated output conductor (FIG.4 TDO). And in view of the motivation previously stated, the claim is rejected.

8. Claims 8, 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jabar, U.S. Patent No. 6028983, and in view of Jin, U.S. Patent No. 6266801.

As per Claim 8:

Jaber teaches a system for testing one or more of multiple circuit modules embedded in an integrated circuit (see Abstract), comprising: a test controller for accepting serial data and control signals from outside the integrated circuit in accordance with a test protocol that corresponds to a board level test protocol (FIG.5 39), the controller including; a first selector for selecting one of the multiple circuit

modules for testing (FIG.5 47), control signals being transmitted to only the selected one of the test modules (FIG.5 49, 51); and a second selector for selecting output from the selected one of the circuit modules (FIG.5 53); and a boundary scan register corresponding to each of the one or more circuit modules (FIG.5 SCAN STRING 0...n), the boundary scan register providing input to circuit modules from the controller in a test mode and from an operating input when in operating mode (FIG.7 70 and FIG.6 DATA IN). However, Jaber fails to teach distribution of four signals in this manner to comply with other master/slave scan register designs. In an analogous art, Jin does teach the feature, using multiple sets of four conductors (FIG.1C, MODE, SHIFTDR, CLOCKDR, UPDATEDR, as well as FIG.4). One with ordinary skill in the art would find it to be an obvious choice to include the said four conductors in a master/slave arrangement as taught by Jin into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several embedded circuits within an integrated circuit. Jin, in column 2 lines 63-66 and column 2 lines 1-6 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's timing characteristics in order to serve several core circuits. One with ordinary skill in the art at the time of the invention, motivated by Jin, would combine the two references in order to control several core circuits, thus the claim is rejected.

As per Claim 9:

Jaber further teaches the system of claim 8 in which the test controller includes logic for using serial data and control signals in accordance with a JTAG protocol

(column 4 lines 8-13). And in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

Jaber fails to further teach distribution of four signals to comply with other master/slave scan register designs. In an analogous art, Jin does teach the feature, using multiple sets of four conductors (FIG.1C, MODE, SHIFTDR, CLOCKDR, UPDATEDR, as well as FIG.4). One with ordinary skill in the art would find it to be an obvious choice to include the four conductors in a master/slave arrangement as taught by Jin into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several embedded circuits. Jin, in column 2 lines 63-66 and column 2 lines 1-6 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's timing characteristics while serving several core circuits. One with ordinary skill in the art at the time of the invention, motivated by Jin, would combine the two references, thus the claim is rejected.

As per Claim 12:

Jaber further teaches the system of claim 8 further comprising a data input line that connects from the test controller to every boundary scan register (FIG.5 TDI). And in view of the motivation previously stated above, the claim is rejected.

As per Claim 13:

Jaber further teaches the system of claim 8 further comprising multiple data output lines (FIG.5 SCAN STRING 0...n), each connecting from a different boundary

scan register to the second selector (FIG.5 53). And in view of the motivation previously stated above, the claim is rejected.

9. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jabar, U.S. Patent No. 6028983, and in view of Sim, U.S. Patent No. 6374380. Jaber further teaches the system of claim 8 in which each boundary scan register includes test logic for each input pin (FIG.5 47 and SCAN STRING 0...n) output pin (FIG.5 49, 51 and SCAN STRING 0...n), of the corresponding circuit module, the test logic for each input or output pin including a latch for scanning in data (FIG.5 m of each scan string), and a latch for applying data (FIG.5 s of each scan string). Jaber fails to teach a bi-directional pin, a tri-state buffer, and a data selector for selectively conveying data from the latch to the input pin. In an analogous art, Sim teaches these features in FIG.8 (selector 66) and bi-directional circuit in FIG.11, as well as being a tri-state buffer (column 2 lines 45-48). One with ordinary skill in the art would find it to be an obvious choice to add a bi-directional capability arrangement as taught by Sim into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several types embedded circuits, including bi-directional types. Sim, in column 2 lines 1-49 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's I/O pin overhead. One with ordinary skill in the art at the time of the invention, motivated by Sim, would combine the bi-directional and tri-state circuits to Jabar in order to serve several types of embedded circuits, thus the claims are rejected.

Conclusion

Of the pending Claims 1, 3-9, 11-18, 23 and 24:

Claims 23 and 24 are maintained as being rejected under 35 USC 103 as per the examiner's previous office action.

Claims 1, 3-9, and 11-18 are rejected under 35 USC 103 as outlined above in this action.

All pending Claims 1, 3-9, 11-18, 23 and 24 stand rejected.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (703)

272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P. Trimmings

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Guy J. Lamarre

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